PCH2542

User's Manual

Beijing ART Technology Development Co., Ltd.

Contents

Chapter 1 Overview

PCH2542 is a Counter card based on PC104+ bus. It can be directly connected with PC104+ interface of computer to constitute the laboratory, product quality testing center and systems for different areas of data acquisition, waveform analysis and processing. It may also constitute the monitoring system for industrial production process.

Unpacking Checklist

Check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the local dealer or sales for a replacement. Retain the shipping carton and packing material for inspection by the dealer.

Check for the following items in the package. If there are any missing items, contact your local dealer or sales.

- PCH2542 Data Acquisition Board
- ART Disk
    a) user's manual (pdf)
    b) drive
   c) catalog
- Warranty Card

FEATURES

- Isolation Voltage: 2500V
- 32-bit Counter/Timer, 9 independent subtraction counters
- Count Mode: 6 modes
- Input Electrical Standards (O.CLKn, O.GATEn, n=0~8): low level $\leqq 0.8V$, high level $\geqq 2V$
- Output Electrical Standards (O.OUTn): low level $\leqq 0.5V$, high level $\geqq 2.4V$
- Clock Source (O.CLKn): frequency range 1Hz~10MHz
- Gate (O.GATEn): rising edge, high level, low level
- Counter Output (O.OUTn): high level, low level
- Operating Temperature Range: 0℃~50℃
- Storage Temperature Range: -20℃~70℃

Other Features

Dimension: 90.3mm (L)*96mm (W) *16mm (H)

Chapter 2 Components Layout Diagram and a Brief Description

2.1 The Main Component Layout Diagram
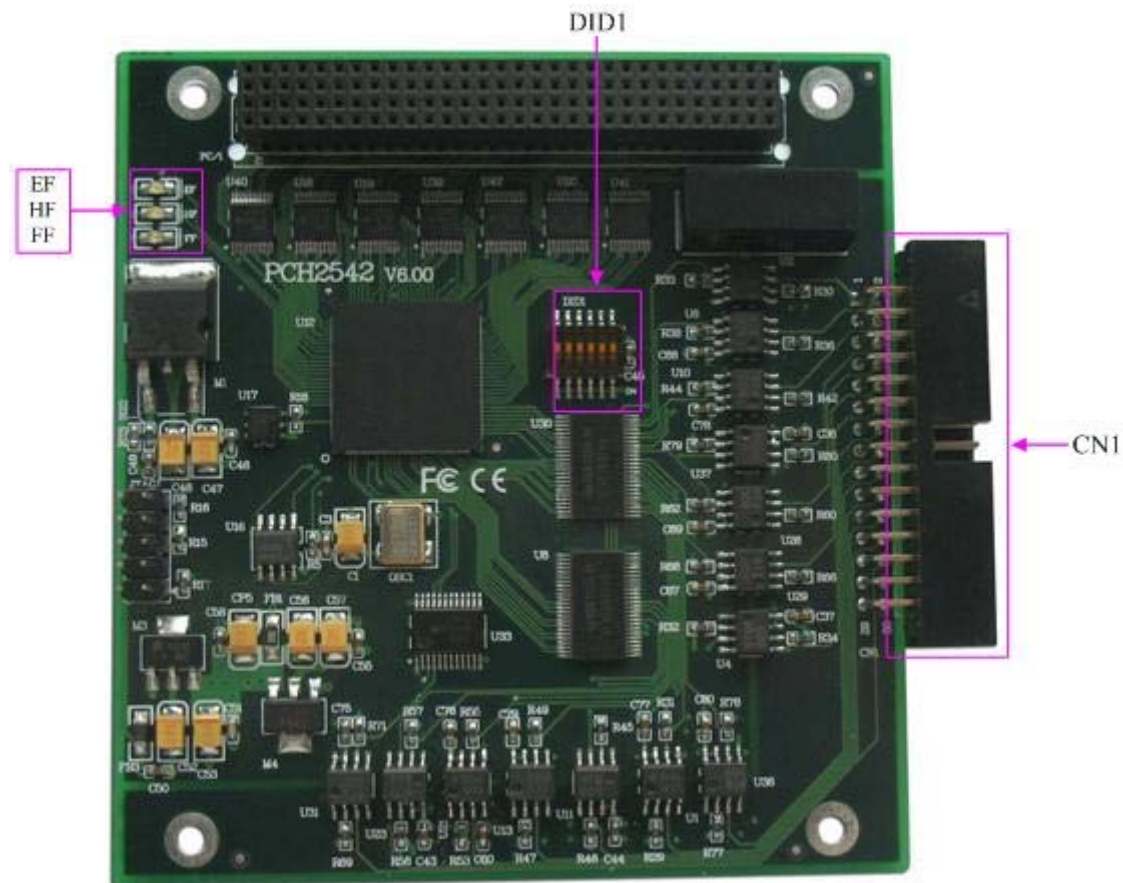
2.2 The Function Description for the Main Component

### 2.2.1 Signal Input and Output Connectors

CN1: signal input/output connector

### 2.2.2 Board Layer and Physical ID Selection

DID1: set the board ID and physical layers, switch No. 1, 2, 3, 4, 5, 6 correspond to ID0, ID1, ID2, ID3, ID4, ID5.

ID0, ID1, are board layer setting, when install multiple PC104+ boards, the board is inserted in the PC104+ interface is the bottom board, the layer number is 0, the boards up from the bottom to the up, the layer number is 1,2,3. The ID2 ~ ID5 is the physical ID setting, when install multiple PCH2542, we can use the DIP switches to set each one PCH2542 physical ID number, then the users can easily distinguish and access each card by the hardware configuration and software programming.

Switch ID2, ID3, ID4, ID5 are physical ID number setting, each bit is the binary, switches dial to "ON" that means the 1, the switch to the other side means 0. (When the board left the factory, the test software usually uses the logical ID to management device, so the physical ID is invalid. If you want to use multiple devices in a system, we had better to use physical ID.)
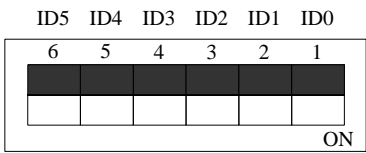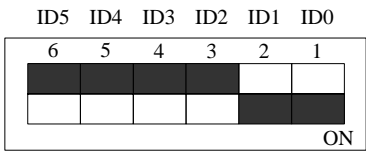
ID5	ID4	ID3	ID2	ID1	ID0
6	5	4	3	2	1

The figure indicates "000000", the layer number is 0, and the physical ID number is 0

ID5	ID4	ID3	ID2	ID1	ID0
6	5	4	3	2	1
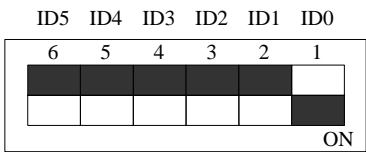
The figure indicates "000001", the layer number is 1, and the physical ID number is 0

ID5	ID4	ID3	ID2	ID1	ID0
6	5	4	3	2	1
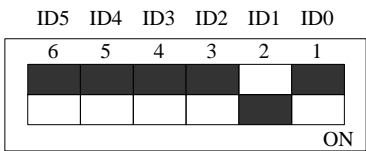
The figure indicates "000010", the layer number is 2, and the physical ID number is 0

ID5	ID4	ID3	ID2	ID1	ID0
6	5	4	3	2	1

The figure indicates "000011", the layer number is 3, and the physical ID number is 0

The table is the layer number setting

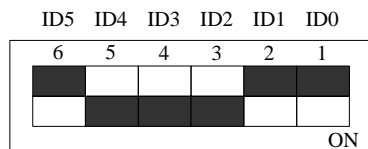| ID1	ID0	Layer Number
OFF（0）	OFF（0）	0
OFF（0）	ON（1）	1
ON（1）	OFF（0）	2
ON（1）	ON（1）	3
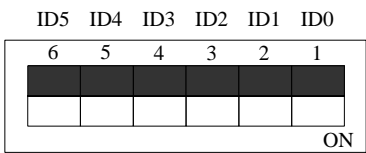
ID5	ID4	ID3	ID2	ID1	ID0
6	5	4	3	2	1

The figure indicates "000000", the layer number is 0, and the physical ID number is 0

ID5 ID4 ID3 ID2 ID1 ID0

| 6 | 5 | 4 | 3 | 2 | 1 |

ON

The figure indicates "010100", the layer number is 0, and the physical ID number is 5

ID5 ID4 ID3 ID2 ID1 ID0

| 6 | 5 | 4 | 3 | 2 | 1 |

ON

The figure indicates "011100", the layer number is 0, and the physical ID number is 7

ID5 ID4 ID3 ID2 ID1 ID0

| 6 | 5 | 4 | 3 | 2 | 1 |

ON
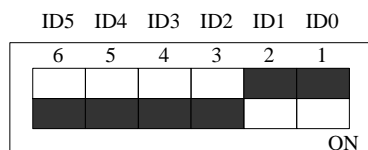
The figure indicates "111100", the layer number is 0, and the physical ID number is 15

Physical ID setting

ID5	ID4	ID3	ID2	Physical ID（Hex）	Physical ID（Dec）
OFF（0）	OFF（0）	OFF（0）	OFF（0）	0	0
OFF（0）	OFF（0）	OFF（0）	ON（1）	1	1
OFF（0）	OFF（0）	ON（1）	OFF（0）	2	2
OFF（0）	OFF（0）	ON（1）	ON（1）	3	3
OFF（0）	ON（1）	OFF（0）	OFF（0）	4	4
OFF（0）	ON（1）	OFF（0）	ON（1）	5	5
OFF（0）	ON（1）	ON（1）	OFF（0）	6	6
OFF（0）	ON（1）	ON（1）	ON（1）	7	7
ON（1）	OFF（0）	OFF（0）	OFF（0）	8	8
ON（1）	OFF（0）	OFF（0）	ON（1）	9	9
ON（1）	OFF（0）	ON（1）	OFF（0）	A	10
ON（1）	OFF（0）	ON（1）	ON（1）	B	11
ON（1）	ON（1）	OFF（0）	OFF（0）	C	12
ON（1）	ON（1）	OFF（0）	ON（1）	D	13
ON（1）	ON（1）	ON（1）	OFF（0）	E	14
ON（1）	ON（1）	ON（1）	ON（1）	F	15

2.2.3 Status Lights

EF: FIFO non-empty indicator, ON is non-empty status.

HF: FIFO half-full indicator, ON is half-full status.

FF: FIFO overflow indicator, ON is overflow status.

Chapter 3 Signal Connectors

3.1 The Definition of Signal Input and Output Connectors

30-pin CN3 definition

O.CLK0	1	2	O.GATE0
O.OUT0	3	4	O.CLK1
O.GATE1	5	6	O.OUT1
O.CLK2	7	8	O.GATE2
O.OUT2	9	10	O.CLK3
O.GATE3	11	12	O.OUT3
O.CLK4	13	14	O.GATE4
O.OUT4	15	16	O.CLK5
O.GATE5	17	18	O.OUT5
O.CLK6	19	20	O.GATE6
O.OUT6	21	22	O.CLK7
O.GATE7	23	24	O.OUT7
O.CLK8	25	26	O.GATE8
O.OUT8	27	28	+5V
O.GND	29	30	O.GND

Pin definition:

Pin name	Type	Pin function definition
O.CLK0~8	Input	Timer/Counter clock source input, the reference ground use O. GND
O.GATE0~8	Input	Timer/Counter gate input, the reference ground use O. GND
O.OUT0~8	Output	Timer/Counter output, the reference ground use O. GND
+5V	Output	Output +5V power
O.GND	GND	Digital ground

3.2 Timer/Counter Signal Connection
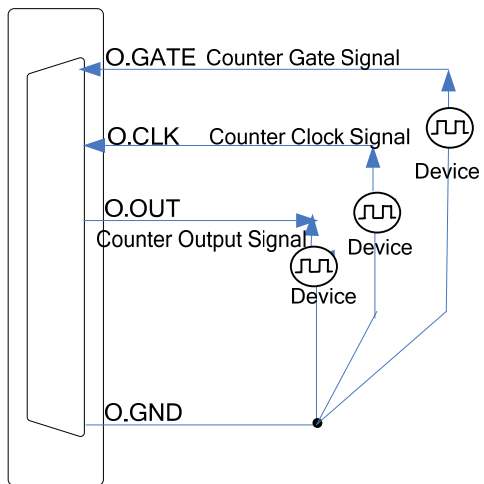
Chapter 4 Timer/Counter Function

Mode 0: Interrupt on terminal count

Under this mode, when given the initial value, if GATE is high level, the counter immediately begins to count by subtracting "1" each time, the counter output OUT turns into low level; when the count ends and the count value becomes 0, the counter output OUT becomes and keeps high level until given the initial value or reset. If a counter which is counting is given a new value, the counter will begin to count from the new value by subtracting "1" each time. GATE can be used to control the count, GATE=1 enables counting; GATE=0 disables counting.

OUT signal changes high from low can be used as interrupt request.

Time diagram is shown in Figure 1.
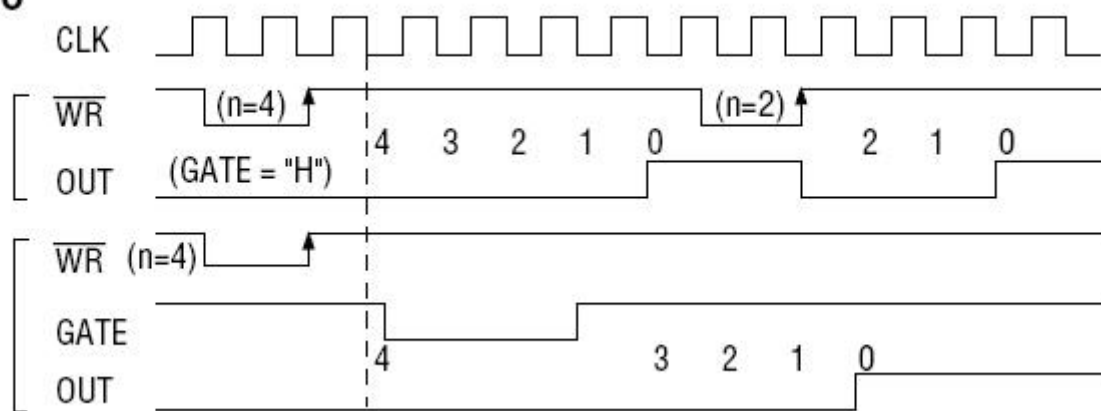
Figure 1

Mode 1: Hardware retriggerable one-shot

The mode can work under the role of GATE. After given the initial count value N, OUT becomes high level, the counter begins to count until the appearance of the rising edge of GATE, at this moment OUT turns into low level; when the count ends and the count value becomes 0, OUT becomes high level, that is, the output one-shot pulse width is determined by the initial count value N. If the current operation does not end and another rising edge of GATE appears, then the current count stops, the counter begins to count from N once again, and then the output one-shot pulse will be widened. When the count reduction of the counter has not yet reached zero, but it is given a new value N1. Only when it is the rising edge of GATE, the counter starts to count from N1.

Time diagram is shown in Figure 2.

Mode 1

Figure 2

Mode 2: Rate Generator

Under this mode, the counter is given the initial count value N and begins to count from (N-1), OUT becomes high level. When the count valu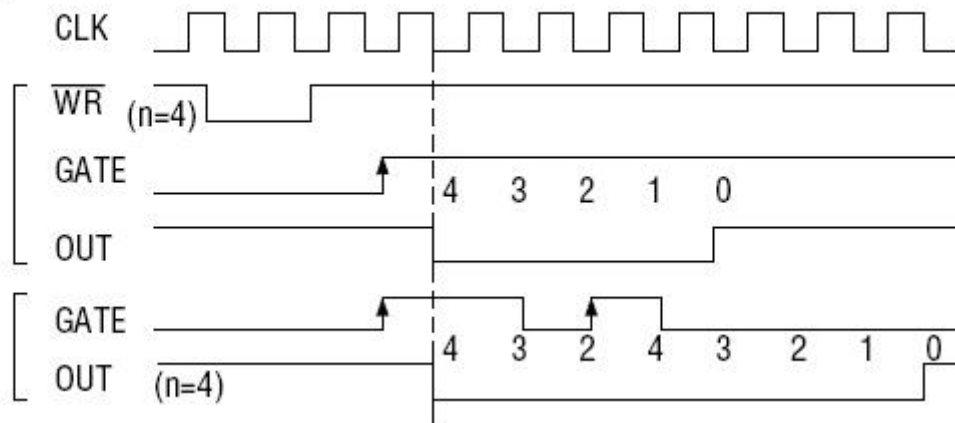e becomes 0, OUT turns into low level. After a CLK cycle, OUT resumes high level, and the counter automatically load the initial value N and begin to count from (N-1). Thus the output will continue to output a negative pulse, its width is equal to one clock cycle, the clock number between the two negative pulses is equal to the initial value that is given to the counter. GATE=1 enables counting; GATE=0 disables counting. GATE has no effect on OUT. If change the initial count when counting, it will be effective next time.

Time diagram is shown in figure 3.
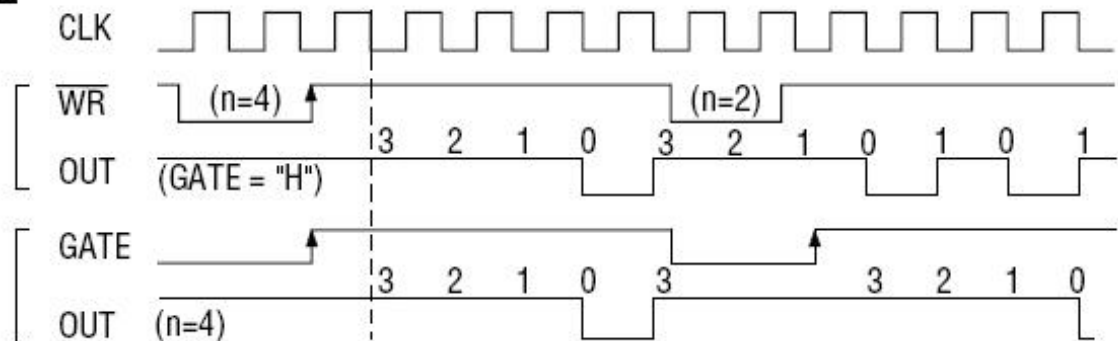
Figure 3

Mode 3: Square wave mode

Similar to Mode 2, the counter is given the initial count value N and begins to count from (N-1). When the signal of GATE is high level, it starts to count, timer/counter begins to count by subtracting "1" each time, more than half the initial count value. The output OUT has remained high level, when the count value is more than half of the initial count value; but the output OUT becomes low level, when the count value is less than half of the initial value. If the initial count value N is an even number, the output is 1:1 square-wave; if the initial count value N is an odd number, the output OUT has remained high level during the previous (n +1)/2 count period; but the output OUT becomes low level during the post (n-1)/2 count period, that is, the high level has one clock cycle more than the low level. If change the initial

count when counting, it will be effective next time. When GATE = 0, the count is prohibited, when GATE = 1, the count is permitted. Time diagram is shown in figure 4.

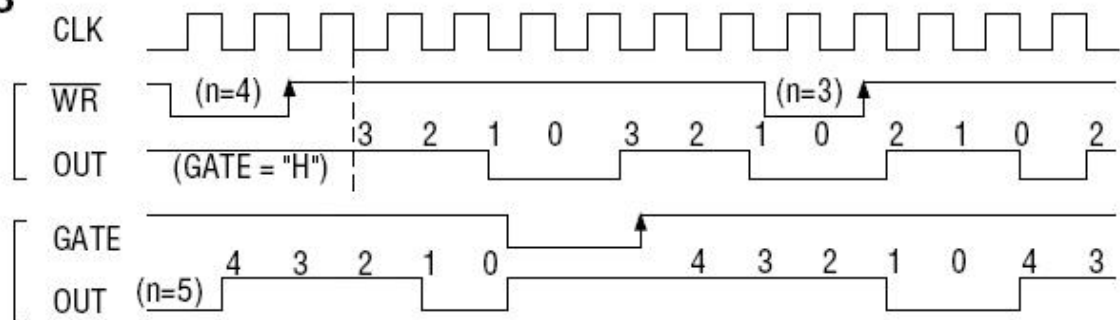Figure 4

Mode 4: Software triggered strobe

Under this mode, the counter is given the initial count value N and begins to count, the output OUT becomes high level. When the count value becomes 0, it immediately outputs a negative pulse which is equal to the width of one clock cycle. If given a new count value when counting, it will be effective immediately. GATE=1 enables counting; GATE=0 disables counting. GATE has no effect on OUT. Time diagram is shown in figure 5.
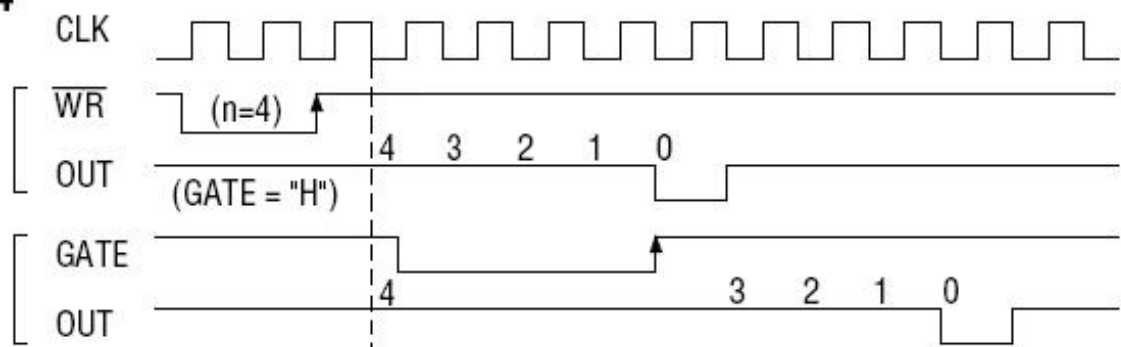
Figure 5

Mode 5: Hardware triggered strobe

Under this mode, when the signal of GATE is on the rising edge, the counter starts to count (so it is called hardware trigger), the output OUT has remained high level. When the count value becomes 0, it outputs a negative pulse which is equal to the width of one clock cycle. And then the rising edge of GATE signal can re-trigger, the counter starts to count from the initial count value again, in the count period, the output has remained high level. When the count reduction of the counter has not yet reached zero, but it is given a new value N1. Only when it is the rising edge of GATE, the counter starts to count from N1. Time diagram is shown in figure 6.

Mode 5

Figure 6

Chapter 5 Notes, Calibration and Warranty Policy

5.1 Notes

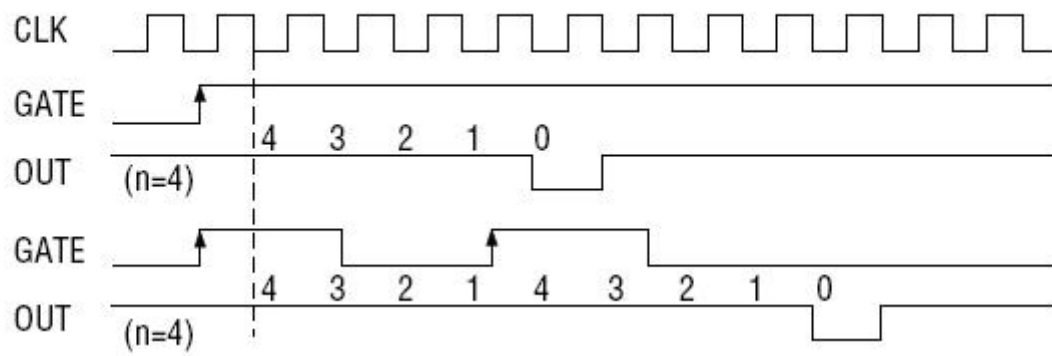In our products' packing, user can find a user manual, PCH2542 module and a quality guarantee card. Users must keep quality guarantee card carefully, if the products have some problems and need repairing, please send products together with quality guarantee card to ART, we will provide good after-sale service and solve the problem as quickly as we can. When using PCH2542, in order to prevent the IC (chip) from electrostatic harm, please do not touch IC (chip) in the front panel of PCH2542module.

5.2 Warranty Policy

Thank you for choosing ART. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ART's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: www.art-control.com.

2. All ART products come with a limited two-year warranty:

➢ The warranty period starts on the day the product is shipped from ART's factory

➢ For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ART is not responsible for any loss of data.

➢ Please ensure the use of properly licensed software with our systems. ART does not condone the use of pirated software and will not service systems using such software. ART will not be held legally responsible for products shipped with unlicensed software installed by the user.

3. Our repair service is not covered by ART's guarantee in the following situations:

➢ Damage caused by not following instructions in the User's Manual.

➢ Damage caused by carelessness on the user's part during product transportation.

➢ Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).

➢ Damage from improper repair by unauthorized ART technicians.

➢ Products with altered and/or damaged serial numbers are not entitled to our service.

4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.

5. To ensure the speed and quality of product repair, please download an RMA application form from our company website.

Products Rapid Installation and Self-check

Rapid Installation

Product-driven procedure is the operating system adaptive installation mode. After inserting the disc, you can select the appropriate board type on the pop-up interface, click the button【driver installation】; or select CD-ROM drive in Resource Explorer, locate the product catalog and enter into the APP folder, and implement Setup.exe file. After the installation, pop-up CD-ROM, shut off your computer, insert the PCI card. If it is a USB product, it can be directly inserted into the device. When the system prompts that it finds a new hardware, you do not specify a drive path, the operating system can automatically look up it from the system directory, and then you can complete the installation.

Self-check

At this moment, there should be installation information of the installed device in the Device Manager (when the device does not work, you can check this item.). Open "Start -> Programs -> ART Demonstration Monitoring and Control System -> Corresponding Board -> Advanced Testing Presentation System", the program is a standard testing procedure. Based on the specification of Pin definition, connect the signal acquisition data and test whether AD is normal or not. Connect the input pins to the corresponding output pins and use the testing procedure to test whether the switch is normal or not.

Delete Wrong Installation

When you select the wrong drive, or viruses lead to driver error, you can carry out the following operations: In Resource Explorer, open CD-ROM drive, run Others-> SUPPORT-> PCI.bat procedures, and delete the hardware information that relevant to our boards, and then carry out the process of section I all over again, we can complete the new installation.